Design of a Kogge Stone Adder Using CNTFETs

P. Gokul, J. HariRajKumar

Abstract—Faster operation and lower power are the most critical parameters in the electronic chip design and is the need of the present-day technologies as well. The addition operation is the most basic arithmetic operation in almost all the digital signal-processing applications. Therefore, an adder should consume only a small fraction of processor's time to be efficient. In this paper, a high speed 16 bit Kogge Stone Adder is designed based on 32nm CNTFET technology using HSPICE. In order to reduce area issues that are usually associated with the high-performance adder designs, CNTFET is chosen.

Index terms—Carbon Nanotube Field-Effect Transistors, 16 bit Kogge Stone Adder, Parallel prefix adder and Low power.

1 INTRODUCTION

The Parallel Prefix Adders (PPA) are very useful in today's world of technology because of their extensive use in the chip design. The Very Large Scale Integration (VLSI) chips depend immensely on fast and unfailing arithmetic operations. The PPAs can fulfill these requirements [1]. The Kogge Stone Adder is a parallel prefix form of the carry lookahead adder (CLA). The Kogge Stone Adder generates the carry in O (log n) time, is widely portrayed as the fastest adder available, and is largely used in the high-performance arithmetic circuits. In this adder, carries are computed faster by computing them in parallel at the expense of area [1].

The semiconductor industry has witnessed an exponential growth in the number of transistors on every integrated circuit for several decades, as forecasted by Moore's law. Silicon devices do not prove proficient at scaled domains because of the sub-threshold voltage problems and short channel effects that come up when the devices are scaled down to sub-nanometer range. A material that was found to surmount the above mentioned problems in the nanometer range (sub ~22nm) is the Carbon material and a range of devices were developed in the nano domain like FinFETs, carbon nanotube field-effect transistor (CNTFETs) etc. Among all these devices, Carbon Nanotubes (CNTs) are seen as the potential replacements for the conventional Silicon transistor technology.

- *P. Gokul is currently pursuing masters degree program in VLSI Design in Sona College of Technology Salem, Tamil Nadu, India. E-mail: prithivgokul@gmail.com.*
- *Prof. J. HariRajKumar is currently working as an Associate Professor in the Department of Electronics and Communication Engineering (PG) at Sona College of Technology Salem, Tamil Nadu, India. E-mail:harirajkumar@gmail.com.*

Carbon in its semiconductor form exhibit a mobility which is ten folds greater than the Silicon materials due to its ballistic transport and OFF-current properties [2], [3]. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT [4]. Therefore, a multi-threshold design can be realized by employing CNTs with different diameters in the case of CNTFETs. The mobility of holes and electrons are almost the same in the case of the Carbon Nanotube based Field-Effect Transistors. Therefore, the operation is expected to be faster in the designs using CNTs compared to the designs using Silicon technology.

This paper is organized as follows. The modeling of Carbon Nanotube for the transistor applications is presented in the Section 2. A description about the Parallel Prefix Adder is given in the section 3. The details about the construction of the 16 bit Kogge Stone Adder is given in the section 4. Results and discussions are made in the Section 5.

2 CARBON NANOTUBE TRANSISTOR MODEL

Carbon Nanotube was discovered accidentally as a byproduct in the carbon cathode used in the arc-discharging process for preparing fullerenes. The origin of CNTs actually started from fullerenes as a hollow spherical structure of an allotrope of carbon C_{60} [4]. The spherical structure is also referred as buck minster fullerene or buckyball, which is shown in Fig.2. Carbon nanotubes, which are the extended structure of a fullerene, are composed of ultrathin carbon fiber with a diameter in the nanometer range and length in the micrometer range. When their hexagonal structures are orientated differently, we have a range of structures like armchair, chiral and zigzag structure coming up and this property allows the CNTs to behave like metal, semiconductor and insulator in the same order as the structures are mentioned [4]. Therefore, these characteristics are employed in semiconductor industries for the development of the CNT based Field-Effect Transistors.

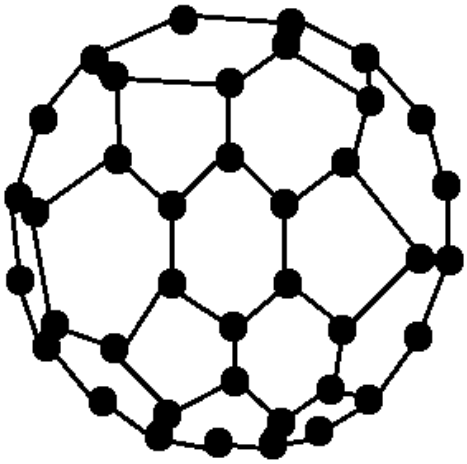

Fig. 1. Buckyball C_{60}.

The orientations can be determined by a measurement factor termed as the chiral vector. Using these orientational advantages that are associated with the CNTs along with their different conducting natures, CNTFETs were developed. Being one of the reliable new transistors, CNTFETs overcomes most of the fundamental limitations coupled with the traditional silicon MOSFETs. The CNTFETs have diverse modeling parameters and factors; some of them are discussed in this section. The Structure of a CNTFET is shown the Fig. 2. Here, channel region in CNT is undoped, while the other regions are heavily doped, acting as both the source or drain extension region and/or as the interconnects between two adjacent devices (the uncontacted source-gate or gate-drain configurations). Nanotube diameter and nanoarray pitch determines the performance and area of a carbon nanotube transistor. CNTFETs make use of semiconducting single-wall CNTs (SWCNTs) to develop electronic devices. An SWCNT can act as either a conductor or a semiconductor, depending on the angle in which the atoms are arranged along the tube. This is referred to as the chirality vector and is denoted by the integer pair (n, m) [5]. As the chirality vector changes, the threshold voltage of the CNTFET will also change. The strength of a CNTFET is varied by changing the number of tubes that form the channel. The CNTFET model which is utilized in this design is the Stanford CNTFET model with a Channel length of 32nm (Lg=32nm). The Stanford CNTFET model was designed for unipolar, MOSFET-like CNTFET devices, where each device can have one or more carbon nanotubes (CNTs). Some parameters of the CNTFET device model [8] are shown in the Table.1,

TABLE 1

Parameters of the CNTFET model

Device Parameters	n/p-type CNTFET
Channel Length (Minimum)	~10nm
Channel Length (Maximum)	Unlimited
Channel Width (Minimum)	4nm
Channel Width (Maximum)	Unlimited

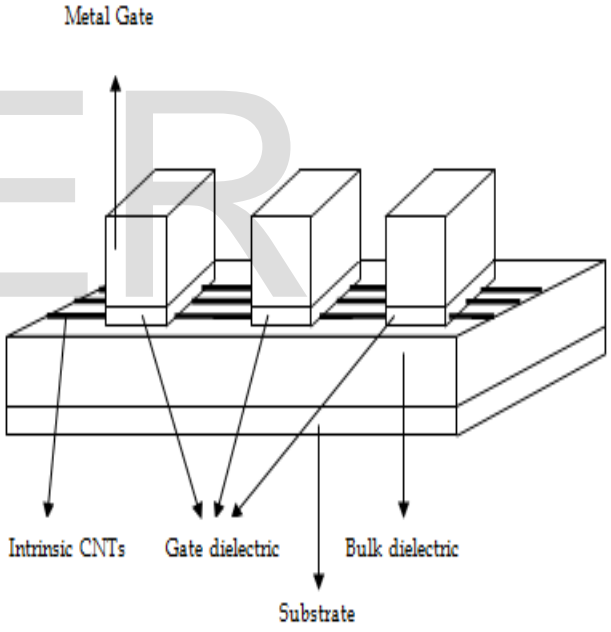

Fig. 2. Three-dimensional device structure of CNTFETs

3 PARALLEL PREFIX ADDERS (PPA)

Fig. 3 illustrates the various stages in the operation of a PPA. PPA has three main stages of operation, namely the pre-processing, group generate and group propagate for

carry graph and post-processing stage [1]. The pre-processing part will produce the propagate (p) and generate (g) bits. The method in which the carry bit is conceived from the previous stages to form the next carry

out differentiates PPAs from other types of adders. Here the carries are obtained in a parallel manner, which enables it to perform addition arithmetic faster. There are different types of PPAs available at the present with each having its own advantages and disadvantages. The most common types of the PPA are Brent-Kung Adder (BKA) and Kogge Stone Adder (KSA) [3].

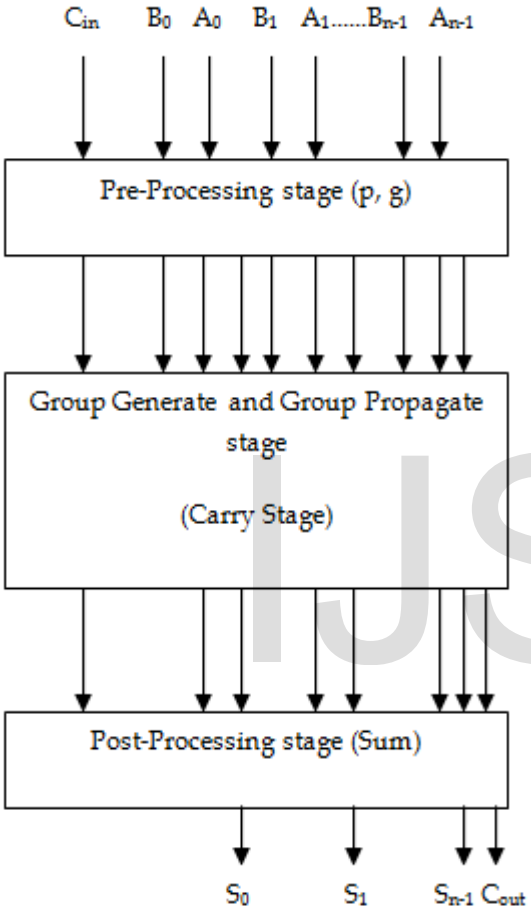

Fig .3. Stages in PPA

In the case of the BKA, the number of levels (or) stages are high, which makes the addition operation a time-consuming process, and it has high fan-out. The Kogge Stone Adder, on the other hand, has a regular layout, which makes them favored adder in the electronic industry comprising of a number of digital signal processing applications [6]. Another reason why a KSA is the preferred over other adders is due of its minimum fan-out or minimum logic depth. Because of these reasons, the KSA becomes the fastest adder among all the adders available not just against Brunt Kung Adder alone [1]. On the other hand, Kogge Stone Adder also suffers from larger device footprint problems that are generally associated with the high-performance adders but with the usage of CNTFETs in this design, the area is expected to be reduced because of the smaller size to which the CNTFETs are fabricated and also the speed is expected to be improved taking into account the mobility of the carriers. The KSA is the parallel prefix form of the Carry Lookahead Adders wherein a lookahead (CLA) network is used to sense whether carry will be generated or not from a particular stage. In the case of the CLA, the different operation is quite the same as PPAs which is as follows,

$$G_i = A_i \text{ or } B_i \quad (1)$$

$$P_i = A_i \text{ and } B_i \quad (2)$$

$$C_{i+1} = G_i \text{ or } (P_i \text{ and } C_i) \quad (3)$$

$$S_i = P_i \text{ xor } C_i \quad (4)$$

Since KSA is a parallel prefix form of CLA, the operations remain the same except at the place where parallel prefix operations are carried on.

4 Proposed 16 Bit Kogge Stone Adder

As mentioned in the previous sections, the Kogge Stone adder is a parallel prefix form of the Carry Lookahead adder and the main difference in the operation of the two adders lie in prefix computation part. In the case of the CLA, the carry of a particular stage is computed by the generate and the propagate terms from the previous stages and the present stage represented the equations (5), (6). The operation of the Kogge Stone adder has the following stages,

4.1 Pre-Processing Stage

In this stage, the propagate and the generate terms are computed in a fashion similar to that used in a CLA. The expressions are shown as follows [3],

$$Pi = Ai \text{ xor } Bi \quad (5)$$

$$Gi = Ai \text{ and } Bi \quad (6)$$

The generate term indicates whether the operation on two input bits will generate a carry value '1'or not. At the same time, a propagate term is used to indicate whether the carry will be propagated on to the next stage or not. If the propagate term at a bit position is '1' then the carry will be propagated to the next stage and vice versa.

4.2 Prefix Computation

The main reason behind the faster operation and better performance of Kogge Stone Adder is in its prefix computation operation. This operation generates group terms (Pij, Gij) from (Gi, Pi) and (Gj, Pj) and their corresponding expressions [3] are as follows,

$$P_{i:j} = P_{i:k+1} \text{ and } P_{k:j} \quad (7)$$

$$G_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j}) \quad (8)$$

The operations performed in this stage make the Kogge stone adder one of the fastest adders available. The carry can be computed using the following expressions [3],

$$C_i = G_{i:0} \text{ or } (C_{in} \text{ and } P_{i:0}) \text{ (or) } G_{i:0} \quad (9)$$

4.3 Post-Processing

In this stage, the final sum output of the design is computed by the following expression [3],

$$S_i = P_i \text{ xor } C_{i-1} \quad (10)$$

Thus, a Kogge Stone Adder of any bit length can be designed by making use of the expressions given above. In this design, the input vectors to the adder are A_1~A_{16}, B_1~B_{16} and C_{in}, where as the outputs are S_1~S_{16} and C_{out}. The design has a number of intermediate signals at the beginning like the propagate signal (p_1~p_{16}) and the generate signal (g_1~g_{16}). The propagate and generate signals after passing through the prefix computation part of the design are denoted as (h_1~h_{16}) and (k_1~k_{16}) respectively to represent the group propagate and group generate terms and also to avoid any confusions as the HSPICE tool which is used to design the Kogge stone adder is case insensitive. Hence node naming is critical as it might lead to errors in the final design if proper care is not shown while naming the nodes. The adder is designed in the transistor level using HSPICE. Here every gate in the gate-level structure is replaced by its equivalent transistor level structure or direct transistor level schematics are drafted in order to design the adder in the transistor level. In the case of the design tool, the design simulations involving CNTFETs can be carried out by including the CNTFET library to the Hspice netlist. In this design, CNTFET model used is a 32nm Stanford CNTFET model.

The complete specification of the parameters used in the transistor model can be referred from [8]. The overall block of a 16 bit Kogge Stone adder is shown in Fig.4, where the black boxes indicate the block that generates the group generate, and group propagate terms. The grey boxes indicate the block that generates the group generate term alone. The triangular symbols just pass the values it receives. The circles in the Fig.4 represent the blocks which compute the propagate and generate terms. Finally, the empty boxes represent the sum generation block as represented by the equation (10). The better performance of

Kogge Stone adder is because of its minimum logic depth and bounded fan-out.

5 RESULTS AND DISCUSSIONS

Thus, a Kogge Stone adder is designed with 32nm CNTFET technology using HSPICE software. The netlist was developed for the design in transistor level and the simulati

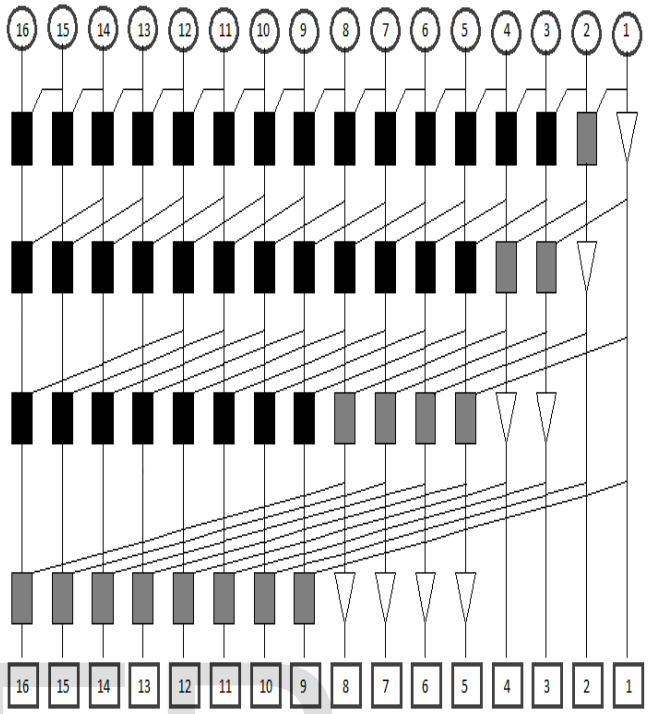

Fig. 4. 16 Bit Kogge Stone Adder

-ons were carried out with a VDD=0.7V [1]. The simulation results were found to coincide with the theoretical results. The simulations were carried out for the following sixteen-bit input vectors in this explanation,

A = 1111111111111111

B = 1111111111111111

Cin = 0

1 1111111111111110

Carry out Sum Bits

The same results were observed in the simulation waveforms. The waveforms for the output S1 to S16 and the

Carry Out are shown in Fig. (5), (6), (7). The Propagation delay and the average power are determined in the design by the inclusion of some additional statements in the HSPICE netlist and the following results were observed,

Average Power = 0.118 µW.

Propagation delay = 0.112 ns.

The Simulation waveforms are shown below,

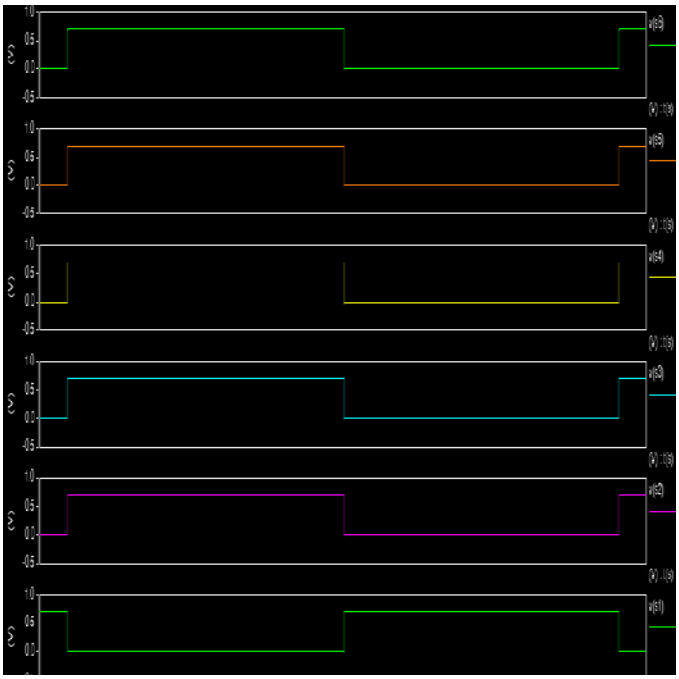

Fig. 5. Output Waveform S1 to S6

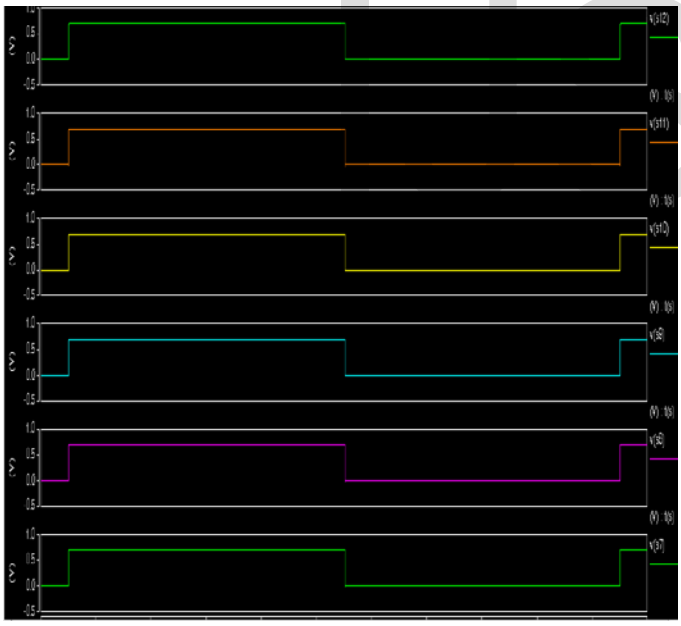

Fig. 6. Output Waveform S7 to S12

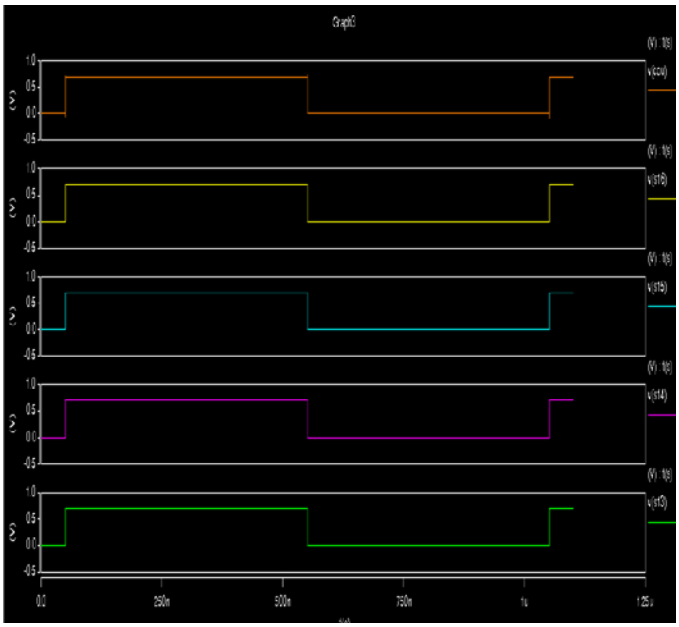

Fig. 7. Output Waveform for S13 to S16 and Cout

6 CONCLUSION

This paper has presented the design of a Kogge Stone adder using CNTFETs. The analysis using the HSPICE tool has shown a very small factor of the power at 0.118µW and the delay value of 0.112ns, which aids to conclude that the adder design using CNTFETs, has a smaller average power as well as a very meager delay. This demonstrates the effectiveness of the Kogge Stone adder designed using CNTFETs. The adder designed is verified for different inputs and the output waveforms generated with the Cosmoscope tool are found to follow the theoretical manual calculations.

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